GB/04/3670

INVESTOR IN PEOPLE

PRIORITY DOCUMENT

SUBMITTED OR TRANSMITTED IN COMPLIANCE WITH RULE 17.1(a) OR (b)

REC'D 28 OCT 2004

WIPO PCT

The Patent Office
Concept House
Cardiff Road
Newport
South Wales
NP10 8QQ

I, the undersigned, being an officer duly authorised in accordance with Section 74(1) and (4) of the Deregulation & Contracting Out Act 1994, to sign and issue certificates on behalf of the Comptroller-General, hereby certify that annexed hereto is a true copy of the documents as originally filed in connection with the patent application identified therein.

I also certify that the attached copy of the request for grant of a Patent (Form 1/77) bears an amendment, effected by this office, following a request by the applicant and agreed to by the Comptroller-General.

In accordance with the Patents (Companies Re-registration) Rules 1982, if a company named in this certificate and any accompanying documents has re-registered under the Companies Act 1980 with the same name as that with which it was registered immediately before re-registration save for the substitution as, or inclusion as, the last part of the name of the words "public limited company" or their equivalents in Welsh, references to the name of the company in this certificate and any accompanying documents shall be treated as references to the name with which it is so re-registered.

In accordance with the rules, the words "public limited company" may be replaced by p.l.c., plc, P.L.C. or PLC.

Re-registration under the Companies Act does not constitute a new legal entity but merely subjects the company to certain additional company law rules.

Signed

Dated 10 September 2004

Patents Form 1/77

Patents Act 1977
(Rule 16)

THE PATENT OFFICE
LJ
28 AUG 2003
RECEIVED BY FAX

The Patent Office

28AU03 E833877-1 D10199
P01/7700 0.00-0320167.0

Request for grant of a patent

(See the notes on the back of this form. You can also get an explanatory leaflet from the Patent Office to help you fill in this form)

The Patent Office

Cardiff Road
Newport
South Wales
NP10 8QQ

1. Your reference — IPMU/2003 012

2. Patent application number *(The Patent Office will fill in this part)* — 0320167.0 — 28 AUG 2003

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

UNIVERSITY OF LEEDS
LEEDS
LS2 9JT

Patents ADP number *(if you know it)* 79832200 1

If the applicant is a corporate body, give the country/state of its incorporation — UK

4. Title of the invention

AN ON-LINE DATA PROCESSING EIT SYSTEM

5. Name of your agent *(if you have one)* (51/77 - 26/3/c

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

~~INTELLECTUAL PROPERTY MANAGEMENT UNIT~~
~~UNIVERSITY OF LEEDS~~
~~3 CAVENDISH ROAD~~
~~LEEDS~~
~~LS2 9JT~~

Harrison Goddard Foote
Fountain Precinct
Balm Green
Sheffield
S1 2JA

Patents ADP number *(if you know it)* ~~[illegible]~~ 79142370 01

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number	Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*
	N/A		

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application	Number of earlier application	Date of filing *(day / month / year)*
	N/A	

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:*

a) any applicant named in part 3 is not an inventor, or
b) there is an inventor who is not named as an applicant, or
c) any named applicant is a corporate body.
See note (d))

YES

Patents Form 1/77

9. Enter the number of sheets for any of the following items you are filing with this form. Do not count copies of the same document

Continuation sheets of this form	–
Description	15
Claim (s)	–
Abstract	–
Drawing (s)	–

10. If you are also filing any of the following, state how many against each item.

Priority documents	–
Translations of priority documents	–
Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	–
Request for preliminary examination and search *(Patents Form 9/77)*	–
Request for substantive examination *(Patents Form 10/77)*	–
Any other documents *(please specify)*	–

11. I/We request the grant of a patent on the basis of this application.

Signature R Wolfson Date 18/8/03

12. Name and daytime telephone number of person to contact in the United Kingdom RAYMOND WOLFSON 0113 3439261

Warning

After an application for a patent has been filed, the Comptroller of the Patent Office will consider whether publication or communication of the invention should be prohibited or restricted under Section 22 of the Patents Act 1977. You will be informed if it is necessary to prohibit or restrict your invention in this way. Furthermore, if you live in the United Kingdom, Section 23 of the Patents Act 1977 stops you from applying for a patent abroad without first getting written permission from the Patent Office unless an application has been filed at least 6 weeks beforehand in the United Kingdom for a patent for the same invention and either no direction prohibiting publication or communication has been given, or any such direction has been revoked.

Notes

a) *If you need help to fill in this form or you have any questions, please contact the Patent Office on 08459 500505.*

b) *Write your answers in capital letters using black ink or you may type them.*

c) *If there is not enough space for all the relevant details on any part of this form, please continue on a separate sheet of paper and write "see continuation sheet" in the relevant part(s). Any continuation sheet should be attached to this form.*

d) *If you have answered 'Yes' Patents Form 7/77 will need to be filed.*

e) *Once you have filled in the form you must remember to sign and date it.*

f) *For details of the fee and ways to pay please contact the Patent Office.*

An online data processing EIT system

FIELD

This invention relates to a device and methods for electrical impedance tomography (EIT), and in particular to a new construction of hardware and software.

BRIEF DESCRIPTION

This patent presents the development of a new Electrical Impedance Tomography (EIT) system for online data acquisition and processing of measurements from two-phase flows, whose axial velocities can be up to 10ms^{-1}, with ±5% precision. To be able to measure two-phase flows at these velocities requires data acquisition speeds (and processing) of 1000 frames/s per dual-plane in order to generate the flow velocity maps. The system has been carefully designed in a modular fashion and can consist of several data acquisition modules and computing modules. The former incorporates a voltage controlled current source with a DC-restore circuit, an over-zero switch circuit, an equal-width pulse synthesizer unit to produce synthetic waveforms for electric field excitation and demodulation signals (for synchronization and sampling) and a synchronized digital demodulation unit with sixteen parallel measurement channels. The computing module incorporates a powerful Digital Signal Processor with an IEEE1394 interface for communication. These modules form a data processing pipeline for a series of tasks ranging from flow measurement to image reconstruction to determining flow velocities. The DSP system can implement three image reconstruction methods, these being the SCG method, the single-step SCG Method and the Back-Projection method. An online-updating cross-correlation algorithm has been developed and is to be implemented on the system. This is particularly suited to flow velocity calculations, as this technique is less time and memory consuming compared to direct cross-correlation techniques. The system architecture, special design techniques, and data processing algorithms will be introduced in the paper along with the current progress in the system's development.

DETAILED DESCRIPTION

The invention will now be illustrated by way of example only with reference to the accompanying drawings, in which

Figure 1 illustrates the system architecture;
Figure 2 illustrates a diagram showing one possible system configuration of high performance two-phase flowmeter using the DSP module as a building block, (a) Single Read-Operation timing, (b) Single Write-Operation timing;
Figure 3 shows the interfaces of Read-timing and Write-timing where t1= 0-60ns; t2=0-252ns, t3=0-12ns. The /CS signal in the figure is chip selection signal decoded from address signal EA[17:2].
Figure 4 illustrates the architecture of the EIT DASsubsystems;
Figure 5 illustrates the structure of Equal-Width Pulse Synthesizer (EWPS);
Figure 6 shows a staircase cosine wave (a) in time domain and (b) in frequency domain;
Figure 7 shows the programmable phase shift function, (a) phase shift 15°, (b) phase shift 45°, (c) phase shift 90°;
Figure 8 illustrates the structure of Synchronised Digital Demodulation (SDD)
Figure 9 shows the configuration of the sampling modes, (a) 4 samplings, (b) 8 samplings, (c) 16 samplings, (d) rolling-sample method;
Figure 10 shows the reading data timing;
Figure 11 shows the sampling signal for measurement timing;
Figure12 shows an equivalent circuit for the EIT transducer electronics;
Figure 13 shows a realization circuit of Over-Current-Zero Switching;
Figure 14 gives a typical curve of the independent measurements obtained from a 2D phantom filled with water. Data was obtained from a 2D phantom filled with mains tap water;

Figure 15 gives an axial cutting image of a high conductive droplet dropped into water, which is stacked from 1000 EIT images reconstructed using SBP algorithm. The 1000 frames of data were taken in 1.06s.

The measurement system can consist of up to four DSP modules, two EIT electrode arrays connected to two EIT Data Acquisition subsystems (DAS's), and a third DAS containing conductivity, pressure, temperature and other auxiliary transducers (as shown in Figure 1).

Control Unit

The control unit is a multi-processor system containing up to four DSP modules. All DSP modules are identical to reduce the design and debugging tasks. The TMS320C6202B is a fixed-point DSP chip with 4 ns instruction cycle time @ 250 MHz clock rate, produced by Texas Instruments, and has been chosen as the processor for the DSP module (Holliday, 2003). Any DSP module can communicate with a remote PC via an IEEE1394 interface. This makes the functionality of any system very flexible. The IEEE1394 interface is fast and can operate over relatively long-distances.

The four modules work on a data pipeline processing technique to increase the data-processing speed. They can perform different tasks on data in pipeline, *e.g*, the first module controls data acquisition and processes raw data; the second module performs image reconstruction and the third module fuses the image data to obtain flow information. A fourth module is provided to carry out other specified functions.

One application that the DSP module is to be used in is the development of a dual plane Electrical Impedance Tomography (EIT) measurement system as outlined in Section 1. This system is required to measure (i) the distribution of local axial, radial and angular velocities of the disperse component, (ii) the distributions of the local volume fraction of both components and (iii) the volumetric flow rate of the disperse component in two component flows. The system has to be able to measure local axial velocities up to $10ms^{-1}$, local radial velocities up to $2.5ms^{-1}$ and angular velocities of up to 45 $rads^{-1}$ with an accuracy of +/-5%. It is expected that the dual plane system will be able to capture 2000 frames/s (1000 frames per plane).

Figure 2 shows a block diagram of how the DSP module could be used to implement such a high performance system. DSP1 acts as the system controller and controls the data acquisition process of two DAS that are connected to it. The DSP then formats the data and transfers it to DSP2. In order to acquire 2000 frames/s, DSP1 has to be able to move 4096 0000 bytes/s from the DAS' using the adjacent electrode data acquisition protocol. The time taken to acquire the 2000 frames is difficult to calculate as the DAS' operate at much slower speeds than the DSP and are autonomous during the measurement process. The data transferred to DSP2 for image reconstruction (data transmitted via McBSP0 on DSP1 and received by McBSP1 on DSP2) will be only 832 000 bytes/s after formatting by DSP1. Besides these tasks DSP1 is also responsible for the IEEE 1394. The McBSP can transfer data at rates up to 12.5Mbyte/s. Therefore if one frame is transferred at a time with 100% overhead this would equate to 67µs per frame allowing plenty of time to transfer 2000 frames in one second. If the data transfer packets were larger then the efficiency of this transfer would increase. Where possible the data transfer operations will be carried out by the DSP's direct memory access controller (DMA). This is an on-board peripheral that is very similar to the DSP's computational processing unit (CPU), but is concerned only with transferring data from one location in the memory map to another without the intervention of the CPU.

DSP2 is charged with implementing the image reconstruction algorithms on the formatted data received from the previous module thus generating image data for each frame acquired by the DAS. The time taken for the image reconstruction for one frame is obtained from the matrix multiplication of a [104x104] matrix by a single 104-column matrix where there are 104 independent measurements and 104 finite elements in the sensitivity map. This gives 10816 multiply-accumulates (MACs). The DSP is capable of 500 million MACs (MMACs) therefore 10816MACs/500MMACs results in a time of 21.6µs per frame. If a generous overhead is added to make this up to 60µs/frame for data accesses then the total time to carry out the image reconstruction for 2000 frames is 100ms.

The image data generated in DSP2 is then transferred to DSP3, again via the McBSP. This module calculates the distribution of the local axial, radial and angular velocities by implementing a moving window of several frames where new image frame data arrives and the oldest image data is destroyed. Determining the time required to carry out the velocity calculations depends on the actual velocity flow. If the axial flow is $10ms^{-1}$ this results in only around 35 frames existing in the frame window. If there are 3 velocity directions and 104 finite elements then one velocity map will take 21.8μs to be calculated. However if we again make this up to 50 μs to cover overhead and apply this to 2000 frames then we have a total time of 100ms. If the two-phase velocity-flow is slower then more frames are used in the velocity calculations. For example if it is $1ms^{-1}$ then 10 times more frames are used. This would take the velocity calculation time up to 1s for 2000 frames. This is at the limit of the systems capabilities, however the more than generous overhead should allow it to be done. In the system proposed the DSP modules will perform their tasks in parallel on a data pipeline. The data acted on in each module is historic in relation to that of the previous module as you move from DSP1 to DSP3.

The DSP External Memory Inter-Face (EMIF) is used to control the DAS's. The related EMIF signals are: EA[17:2]: the low 16 bits of the whole 20-bit address lines, ED[31:0]: 32 bits data lines, /AWE: Asynchronous memory write-enable, /ARE: Asynchronous memory read-enable, /AOE: Asynchronous memory output-enable, TINP0: Timer 0 or general-purpose input, TINP1: Timer 1 or general-purpose input. The read-timing and write-timing from the EMIF, as shown in Figure 3, are similar to that from the PCI bus of a general PC. This simplifies the modular design and debugging. The advantage of the EMIF is that its timings are much faster and more flexible due to its programmability.

EIT DAS subsystems

Two identical EIT DAS's are used in this system to collect data from two electrode arrays or a dual-plane sensor. A block diagram of the EIT DAS is given in the inside of dash-line box in Figure 4. The DAS's is composed from four modules: EWPS, SDD, VCCS and a control base.

An Equal-Width Pulse Synthesizer unit (EWPS) generates a sine-wave voltage signal, which is then converted to two sine-wave currents with a phase difference of 180° by the Voltage Controlled Current Source unit (VCCS). The two currents are used to generate electric fields inside the sensor. The Synchronous Digital Demodulation unit (SDD) measures the electrode voltages and converts these analogue signals to digital data. The digital demodulation design used in this system follows that successfully used by earlier workers (Smith, 1992) that can resolve complex impedances making it suited generally to EIT applications. It then stores all the digital data in a First-In-First-Out memory (FIFO). The data in the FIFO are then transferred into the DSP module via the DSP Direct Memory Access (DMA) function. The SDD and EWPS units are currently designed in a modular format, which may be integrated into three chips in the future, via ASIC design technology. This will minimise the systems physical size and also improve the system performance.

The structure of the EWPS is similar to the widely used Equal-Sample Signal Generator (ESSG). An auto-run clock signal triggers the address generator to continuously output addresses to a pre-written memory. The memory then sequentially outputs data to a Digital-Analogue Converter (DAC). A low-pass filter then smoothes the staircase signal from the DAC to output the required sine-wave voltage signal. The difference between the EWPS and the ESSG is that, the former has different sample numbers at different frequencies to make the stair-case wave using the same time step-length at all frequencies, while the latter has the same number of samples at all frequencies so the stair-case wave has different time step-lengths at different frequencies. This difference has led to a significant reduction in the complexity of the filter design that the EWPS as it only needs to set one corner-frequency for the filter for all signal frequencies while the ESSG needs to set different corner-frequencies for the filter for different signal frequencies. The specially designed EWPS also provides a convenient way to produce a number of synchronized signals that are necessary to carry the required control of the SDD.

16 measurement channels are built into the SDD. Each Channel has one Programmable Gain Amplifier (PGA) and one 12-bit Analogue to Digital converter (A/D). The time and phase of the measurement sampling of the SDD are fully controlled by the synchronous signals from the EWPS.

The A/D conversion and the data transfer to the FIFO are also controlled by a synchronous signal. The measurements can be stacked in the FIFO and collected by the DSP module as block data once the FIFO is full. Compared to the conventional sequential and parallel data collection protocol, not only does this sub-logical controlled data collection protocol significantly shorten the measurement time and eliminate measurement noise caused by the front-end analogue multiplexers, but it also produces a much more accurate sampling time and leaves significant time for DSP to perform other processes.

A smart AD844 based VCCS with DC restoring techniques is used in this system, which has a wide bandwidth, high output impedance, and excellently balanced large output currents (details will be published elsewhere). The two currents are injected into one of 16 pair electrodes via two high-performance analogue multiplexers. An over zero switch (OZS) technique has been designed to eliminate the transient time caused by the residual charge in the coupling capacitance and electrode-electrolyte interface due to the random switching of the excitation currents. By a controlling the switching time (the phase difference to the sine wave signal) using the synchronous signal with a programmable phase provided from the EWPS, the residual potential after the switching is approximately kept is zero.

To collect one frame of raw data, the time cost by a sequential system and the EIT DASs (based on 16 adjacent data acquisition strategy) can be expressed as Equation 1 and 2, respectively.

$$T_{frame} = (T_{sin} \times N_{set} + T_{ADC} + T_{trans}) \times N_{ele}(N_{ele} - 3)/2 \qquad \text{(Equation 1)}$$

$$T_{frame} = (T_{sin} \times N_{set} + T_{ADC} + T_{trans}) \times N_{ele} \qquad \text{(Equation 2)}$$

where N_{ele}: electrode number on one sensing plane, T_{sin}: cycle of the exciting sinusoidal current, N_{set}: cost in terms of cycle numbers for the signal settling, T_{ADC}: acquiring and converting time of the A/D converter, T_{trans}: time used to transfer one A/D result into controlling unit and T_{frame}: time used to collect one frame of raw data.

Assuming T_{sin}=100us (*i.e.* 10kHz exciting frequency), N_{set}=4, T_{ADC}=1.25us, T_{trans}=0.06us, N_{ele}=16, then T_{frame} of the DAS will be 41.73 ms and 6.42 ms respectively. It can be seen that the data acquisition speed is greatly slowed down by the settling time, especially at low exciting frequencies, which is almost linear to the number of signal cycles used for overcoming the settling time. The application of the novel signal conditioner as described above, the N_{set} could be set as one and the most time of T_{frame} would be also available for the data processing in the control DSP, which significantly improves the data collection speed.

Signal conditioner

In previous EIT DAS designs, two digital synthetic (AD7008 DDS) chips were used for sine wave generation and synchronization (Wang 1998). One DDS has been adopted to generate a sine wave, whilst other generates a sampling signal for demodulation. Although the AD7008 can generate a precision sine wave and required sampling signal, the synchronisation between the sine wave and sample signals generated from the two chips are hard to achieve and control. Further, it is also unable to generate a particular waveform, e.g. a synthetic multi-frequency signal, except a sine wave. With the emergence of impedance spectroscopic examinations of materials, a simultaneous spectroscopic technique is becoming desirable (Riu 1995; Shallof 1997).

Equal-Width Pulse Synthesizer (EWPS) is a sine wave voltage generator and synchronous signal generator, as shown in Figure 5. This is composed of a programmable look-up table for the sine wave, a 12 bits Digital to Analogue Converter (DAC), a low pass filter, a 8 bit Digital to Analogue. Converter (DAC) and other logic counting circuits. An oscillator and counter are used to repetitively clock the stored 'staircase' wave out of PROM, which is then converted to analogue waveform by the DAC and the low pass filter. The amplitude of the sine wave can be controlled by a 0 to 1.25 V by an 8 bit DAC. The digital approach can easily generate both the synchronous signal and the sample signal. The synchronous signal (square wave) is used to control of the start of the measurement. The sample signal is a trigger for synchronized digital demodulation.

In the circuit, a PROM-based staircase function generator has been utilised. The PROM is programmed with either a digitised sine wave signal or other particular synthetic waveform staircase, in which the waveform is stored by an equal width step for all different frequencies. In the EWPS operation, the original clock frequency is fixed and unchanging with signal frequency. This uses different sample numbers at different frequencies to make the staircase waveform with the same step-length of time for all frequencies.

It is known that a cosine staircase in the frequency domain can be presented by Equation 3 (Evans 1980).

$$H(f) = \frac{1}{2T}\sum_{k=-\infty}^{+\infty} \Delta[f - (Nk \pm 1)f_0]T \sin c\left(\frac{\pi f}{Nf_0}\right) \qquad \text{(Equation 3)}$$

where N is number of the steps to form a k^{th} frequency and f_0 is the fundamental frequency. The time domain and frequency domain are illustrated in Figure 6.

Considering the use of the same step-length, the sampling pulse frequency, f_s, is unchanged.

$$f_s = Nf_0 \text{ or } f_0 = \frac{1}{N} f_s \qquad \text{(Equation 4)}$$

Therefore,

$$H(f) = \frac{1}{2T}\sum_{k=-\infty}^{\infty} \Delta\left[f - \frac{Nk \pm 1}{N} f_s\right]T \sin c\left(\frac{\pi f}{f_s}\right) \qquad \text{(Equation 5)}$$

Hence, the lowest harmonics from the EWPS is $\frac{N-1}{N} f_s$ and the EWPS may use one low pass filter with a fixed corner frequency for all waveforms. The step-length used in the EWPS is 0.5 μs which gives a sampling pulse frequency of 2.0MHz.

The synchronous signal (square wave) is used to control of the start and end of the sampling and the sampling pulses are triggers for taking a number of measurements in a specific time sequence from an EIT sensor. The timing and width of both signals play a very important role in the achievement of SDD accuracy. Two sampling modes are created by the EWPS. The Mode 1 is 4 to 32 samplings to be selectable per period, and the Mode 2 is a rolling-sample method that performs one sample per period with a fixed phase shift between one and another.

An over zero switch (OZS) technique has been designed to overcome the transient time caused by the residual charge in capacitances in coupling and electrode-electrolyte interface. In order to achieve this function, the multiplexers have to be operated at a precise phase angle. A programmable phase shift (between the synchronised signal and sampling pulses) function is adopted (Wang 1994). This is achieved by the control of the high 8-bits of the PROM address, which selects one of 128 staircase waves with different pre-calculated phase shifts also stored in the PROM. The phase shift can be adjusted from 0° to 90° with a minimum step of 0.703° (see Figure 7).

The Synchronised Digital Demodulator (SDD) is a high speed, synchronised parallel digital demodulation system, which is composed of 16 sets of Programmable Gain Amplifiers (PGA), a 12-bit ADC, a Strobed First-in First-out Memory (FIFO) and control logic. Figure 8 shows the functional block diagram of the SDD.

SDD uses the EWPS sampling signals to acquire the measurement data in parallel at precisely defined intervals. The Mode 1 can acquire 4-32 samples per period with a precise timing. The Mode 2 is particularly designed for sampling at a high frequency due to the speed limitation of the conventional A/D converter. The configuration of the sampling modes is shown in Figure 9. The completion signal of the ADCs with a control clock will then sequentially push the converted data into two FIFO memories. All the operations are logically controlled without the involvement of the DSP, except the starting signal.

Not only the parallel data collection structure can significantly shorten the data collection time but also eliminate measurement noisy caused by front-end analogue multiplexers used in the sequential data collection structure. The required minimum data acquisition time per sample is given as,

$$T_s = T_{ADC} + 8T_R + T_{delay} \qquad \text{(Equation 6)}$$

where T_s is the data acquisition time.
T_{ADC} is data convert time for A/D converter.
T_R is the time for reading the data from A/D converter to FIFO.
T_{delay} is delay time for logic circuit.

Considering all factors, the minimum data acquisition time is about 2 μs, which is shown as Figure 10

The structure of logical control without the involvement of the DSP is a lighting point for the signal conditioner. After the 'start' command is set by DSP, SDD will automatically sample the sensor outputs at precisely defined intervals within one or more periods and convert the analogue data to digital and then, push the digital data into FIFO. The SDD will then return to its initial status (Figure 11). In order to 'inform' the DSP of the working status, a 'busy' signal and a FIFO memory status with the start signal from DSP construct a simple communication interface. This frees up the DSP to perform other tasks as well as shortening the acquisition time.

Conventional, ERT system uses sinusoidal constant current sources to excite the sensing field. Since a controlling unit, such as a PC, DSP or microcomputer, directly controls the current switching between electrodes, the switching operation may occur randomly during anytime of a sinusoidal cycle. When the current value at the time of the switching operation is non-zero, electrical charge may reside in the capacitances of the signal passing circuit, as double layer capacitance, coupling capacitance and stray capacitance. These may result in residual potentials presented between these capacitances and produce an additional contribution to next excitation and measurement. These residual charges will require several sinusoidal cycles to disappear, which means the whole data acquisition system (DAS) has to wait for several cycles after each switching operation in order to perform next voltage measurement. This would be harmful to a parallel measurement structure.

To analyse the effect, an equivalent circuit for one electrode measurement channel is given in Figure 12(a), where C_H is the Helmholtz double layer capacitance, R_c the charge transfer resistance, R_b the bulk resistance, C_C the coaxial cable capacitance and C_S the other stray capacitances (Wang 1994), C_f the AC coupling capacitance (Bockris 1969; Pollak 1974; Wang 1994). Taking typical values of C_H of 10μF/cm^2, R_C of 500Ω.cm^2 (Pollak 1974), C_f of 1μF and R_f of 1MΩ. In the majority of cases, C_S and C_C has a value of around a hundred picoFarads, therefore their effect on the solution is minimal and can be ignored without significantly altering the result.

Assuming the current injection is switched off at t_0, the voltage at the input of the differential amplifier can be expressed as:

$$V_c = \left(\frac{R_C}{1 + j\omega R_C C_H}\right) I_s e^{-t/T_1} e^{-t/T_2} \quad \left(\frac{1}{\omega C_f} << R_f\right) \qquad \text{(Equation 7a)}$$

where $I_{ac} = A\sin(\omega t_0 + \varphi)$, $T_1 = R_c C_H$ and $T_2 = R_f C_f$. (Equation 8)

As $\omega R_c C_H >> 1$, $T_1 << T_2$, then equation 5a can be simplified to:

$$V_{c1} = -j(\omega C_H)^{-1} A e^{-t/T_1} \sin(\omega t + \varphi) = -(\omega C_H)^{-1} A e^{-t/T_1} \cos(\omega t + \varphi) \qquad \text{(Equation 9)}$$

A simplified equivalent circuit and its transient curve are shown in Figure 12(b). Assuming $\omega=20\pi$ kHz, $\varphi=0$, $A=10$ mA, and the current is switched off at $t=t_0=0$, the transient voltages at the input of the differential amplifier should still be 14.4 mV and 5.89 mV in respect to the settling time $\Delta t=0.1T_1$ and $\Delta t=T_1$, ($T_1=0.005$ s). Therefore, the major contribution to the charged residual voltage is from the double layer capacitance, which results a significant drop of the measurement accuracy.

The over-zero switching (OZS) discussed here is aimed to eliminate the charged residual voltage by controlling the switching operation of the current injection. In an ideal case, no charged potential resides in either the double layer capacitance or the coupling capacitance after switching off the current injection so the settling time is shorter with the data acquisition speed being increased. Since the charged voltage has a $\pi/2$ delay with respect to the current, the switch should operated at either zero-voltage between the double-layer capacitance or *maximum-current* through the capacitance. The current-maximum is actually applied to optimise the switching time or the relevant phase difference between the synchronised signal and the sinusoidal signal, as the charged voltage between the double-layer capacitance is hardly measurable.

Figure 13 is the circuit used in the improved system to realize the over-current-zero switching technique. Two inverse-phased currents C1 & C2 are connected to the common inputs of two multiplexers U1 & U2 respectively. 16 electrodes mounted in one sensing plane are connected to the 16 output channels of each multiplexer. Channel selection is together controlled by DSP command and a synchronize signal, SYN_SIN, of current C1. SYN_SIN is a square-wave signal, which has the same over-zero point with two current signals C1 & C2. When DSP send out a switching command, an 8-bits data (each multiplxer is controlled by 4-bits data), ED[0:7], is written into the first flip-flop, U3. This data is later written into the second flip-flop, U4, by the next rising edge of SYN_SIN, and finally make the two multiplxers switch to other channels. A D-type flip-flow, U5A, is used in this circuit to prevent writing data into U4 before the data has been set-up at the output of U3.

Data processing algorithms

Three kinds of image reconstruction algorithms have been coded for the DSP module. They are: SCG method (Wang, 2002), Sensitivity-map-based Back Projection (SBP) method (Kotre, 1994) and a simplified SCG method – Single-step SCG (SSCG) method. The SCG method is a kind of iterative method, which has the highest-performance but is the most complicated and time-consuming of the three. The SSCG method is the SCG method iterated only once from a homogenous conductivity distribution. The SBP method is the simplest and fastest. It seems that the SSCG has a better performance than the SBP method.

The time taken to reconstruct one frame image will be different for each of these algorithms. As an example, the time taken using the SBP reconstruction for one frame is obtained from the matrix multiplication of [104x104] matrix by a single 104-column vector where there are 104 independent measurements and 104 finite elements in the sensitivity map. This gives 10816 multiply-accumulates (MAC). Based on the DSP's capacity of 500 million MACs per second, it needs 21.6 us to complete the matrix multiplication. Adding 100% overhead time, a generous image reconstruction rate of 50us/frame has been calculated. Then the total time to carry out the image reconstruction for 1000 pair of images (2000 frames) would be 100 ms.

Assuming that the two EIT electrode arrays are installed parallel on the flow-pipe, the axial-flow velocity distribution can be estimated by a direct cross-correlation method, as given in Equation 10:

$$R_{12}(n)=\sum_{m=n+1}^{N} f_1(m-n)f_2(m),\ n=0,1,\cdots,(N-1) \qquad \text{(Equation 10)}$$

where N is the sample length, and $f_1(m)$ & $f_2(m)$ are the m^{th} up-flow and down-flow images respectively. Equation 10 can be simply implemented online by updating the $R_{12}(n)$ with the new k-th images, as described in the following:

$$R_{12}^{(k)}(n)=R_{12}^{(k-1)}(n)+f_1(k-n)f_2(k),\ n=0,1,\cdots,(N-1) \qquad \text{(Equation 11)}$$

where superscript *(k)* indicates that the corresponding value is of k-th sample. This implementation can greatly save calculation time and reduce memory size. The computation speed is subject to the number of pairs of images that are estimated as a maximum sampling length. For example take a velocity ranging from 1 m/s to 10 m/s giving a turndown ratio of 10:1 and V_{max}=10m/s, V_{min}=1m/s. Assuming the distance, D, between the two sensing planes in a dual-plane sensor is 0.1 m and the data acquisition speed, V_{acq}, is 1000 frames /sec. the sampling length, N, is 20 frames for V_{max} and 200 frames for V_{min}. The minimum number of multiplications required to find a pixel flow velocity in the velocity range is

$$MAC_{min} = 2 \times \left(\frac{D}{V_{min}} - \frac{D}{V_{max}} \right) \times V_{acq} = 180\,(MAC), \qquad \text{(Equation 12)}$$

which give 37.44μs for generating an axial velocity map with 104 pixels and 50 μs if some overheads are expected. To secure the data accuracy, a repeated computation is normally applied to the sampling window. For a total number of 2000 frames data, it needs 100 ms for the completion of the axial velocity map. According to other workers (Beck, 1986; Wah, 1998), the minimum acquisition time, δ, can be taken as twice the product of the minimum transit time of the fluid, τ, and the fractional velocity discrimination, κ. By rearranging gives the following

$$\kappa = \delta / 2\tau \qquad \text{(Equation 13)}$$

If the distance between two sensing planes is 0.1m then τ = 0.1m/10ms^{-1} = 0.01s. If 1000 frames/s was achieved then δ = 0.001s. Using Equation 6 gives a discriminatory precision of 0.05 or 5%.

Preliminary result

The fast data collection and implementation system has been designed and built at the university of Leeds. A number of trials have been successfully performed. Without making efforts to optimise the control code for data collection, transferring and processing, a data collection rate of 1000 frames per 1.06s was recorded. A 2D phantom fitted with 16 stainless steel electrodes and filled with mains tap water was used in one of the trials. In the experiment, all the PGA's in the SDD were equally set to a fixed gain value in order to simplify the test. The current excitation frequency was 80 kHz. Measurements were taken from all electrodes during each current excitation/projection, which gave 256 measurements. Four samples per period were taken. Therefore, each frame data has a total of 1024 measurements. A simplified digital matched-filter was applied to demodulate the data. A set of independent measurements were then extracted and averaged from their mirror data based on the reciprocal theorem. The new EIT system has not been optimised at the time of carrying the initial test. It is expected that a rate of 1000 pairs (2000 frames) per second could be achieved when two DAS are connected to the system.

The top and middle curves in Figure 14 present two measurements obtained from a vessel filled with mains tap water. The bottom curve denotes the relative change between the two measurements to reflect the repeatability of these measurements. Figure 15 shows an image of a high conductive (100mS) brine droplet (approximately 5ml) injected into a mains tap water background. The image was stacked from 1000 2D images and the droplet was visualised from the axial cutting section of the stacked image. As this is preliminary work, validation of these measurements will be made in the near future and reported on.

REFERENCES

BECK, M.S., PLASKOWSKI, A., (1986) Cross Correlation Flowmeters – their design and application, Adam Hilger, Bristol

Bockris J.O'M and Conway B.E., (1969), *Modern aspects of electrochemistry*, Plenum Press, New York

DAI, Y., MA, Y. and WANG, M., (2003). A specific signal conditioner for electrical impedance tomography, in *Proceedings of World Congress on Industrial Process Tomography*, VCIPT, Banff, Canada

DICKINSON, S.J and PEYTON, A.J, (2001) A high speed, multi-frequency impedance analysing node, *2nd World Congress on Industrial Process Tomography*, pp502-510.

EVANS W.A. AND TOWERS M.S., (1980). Hybird technique in waveform generation and synthesis, IEEE Proc., Vol.127, Pt.G, No.3, pp.119-128

HOLLIDAY, N. T., MA, Y. WANG, M. and WILLIAMS R.A., (2003). A powerful computational DSP module for multiphase flow measurement, in *Proceedings of World Congress on Industrial Process Tomography*, VCIPT, Banff, Canada

KOTRE, C. J. (1994), EIT image reconstruction using sensitivity weighted filtered back-projection, *Physiol. Meas.* 15 A1, pp25-36

LOH, W. W. (1998), *Real-time Monitoring of Drilling Cuttings Transport Using Electrical Resistance Tomography*, Ph.D Thesis, UMIST, pp103-104

MA, Y., HOLLODAY, N., DAI, Y., WANG, M., WILLIAMS, R.A. AND LUCAS G., (2003), A high performance online data processing EIT system, in *Proceedings of World Congress on Industrial Process Tomography*, VCIPT, Banff, Canada

POLLAK V., (1974), Computation of impedance characteristic of metal electrode for biological in vestigations, *Med.and Biolo. Engng.*, pp.460-464

RIU, P.J., ROSELL, J., LOZANO, A. AND PALLAS-ARENY, R., (1995). Multi-frequency static imaging in electrical impedance tomography: Part 1 instrumentation requirements, *Medical & Biological Engineering & Computing*, v 33, 6, pp. 784-792

SHALLOF, A.M., BARBER, DAVID C., (1997). Multifrequency electrical impedance tomography: tissue characterization and image quality, *The International Society for Optical Engineering*, v 3031, pp. 699-707

SMITH, R. W. M, FREESTON, I. L, BROWN B. H. and SINTON A. M., (1992) Design of a phase-sensitive detector to maximize signal-to-noise ratio in the presence of Gaussian wideband noise, *Meas. Sci. Technol.* 3, pp.1054-1062

TII, (2000), *TMS320C6202/B Fixed-Point Digital Signal Processors*, Texas Instruments Incorporated

WAH, L. W., (1998) Real-time monitoring of drilling cuttings transport using electrical resistance tomography, Ph.D. Thesis, UMIST

WANG M. and DICKIN F.J., (1994). Signal phase shift and compensation in resistive electrical impedance tomography' in *Process Tomography - A Strategy for Industrial Exploitation - 1993*, Edited by BECK, M.S., CAMPOGRANDE, E., MORRIS, M., WILLIAMS, R.A. AND WATERFALL, R.C., UMIST, pp. 193-196

WANG M., (1994), *Electrical impedance tomography on conducting walled process vessels*, PhD thesis, UMIST

WANG M., (1998). Recent progresses on ERT instrumentation, Research report in *TFC/TM/STD/10-03-1998/UMA/4012/D/*, UMIST

WANG M (2002) Inverse solutions for electrical impedance tomography based on conjugate gradients methods, *Meas. Sci. & Tech.*, 13, pp.101-117

INDEX OF FIGURES FOR A HIGH PERFORMANCE DATA PROCESSING EIT SYSTEM

Figure 1: System Block Diagram

Figure 2: A diagram showing one possible system configuration of high performance two-phase flowmeter using the DSP module as a building block, (a) Single Read-Operation Timing, (b) Single Write-Operation Timing

Figure 3: Interface Read-Timing And Write-Timing Where t1= 0-60ns; t2=0-252ns, t3=0-12ns. The /CS signal in Fig.2 is chip selection signal decoded from address signal EA[17:2].

Figure 4: Architecture of EIT DAS

Figure 5: The structure of Equal-Width Pulse Synthesizer (EWPS)

Figure 6: A staircase cosine wave (a) in time domain and (b) in frequency domain

Figure 7: Programmable phase shift function, (a) phase shift 15°, (b) phase shift 45°, (c) phase shift 90°;

Figure 8: The structure of Synchronised Digital Demodulation (SDD)

Figure 9: The configuration of the sampling modes, (a) 4 samplings, (b) 8 samplings, (c) 16 samplings, (d) rolling-sample method

Figure 10: Reading data timing

Figure 11: Sampling signal for measurement timing

Figure12: An equivalent circuit for the EIT transducer electronics

Figure 13: A typical curve of the independent measurements obtained from a 2D phantom filled with water. Data was obtained from a 2D phantom filled with mains tap water.

Figure 14: An axial cutting image of a high conductive droplet dropped into water, which is stacked from 1000 EIT images reconstructed using SBP algorithm. The 1000 frames of data were taken in 1.06s

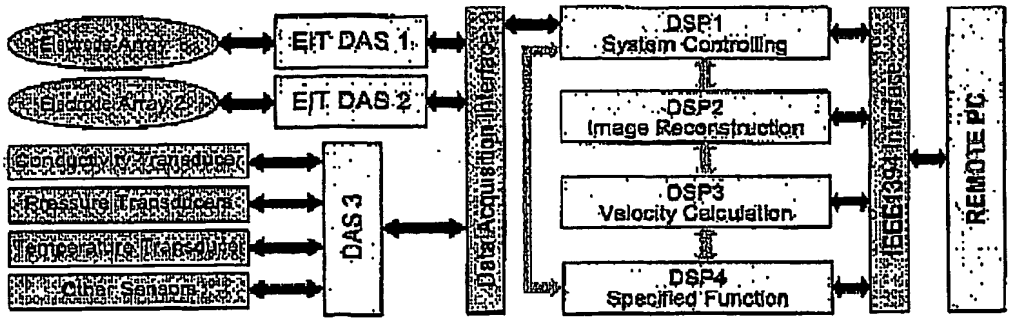

Figure 1: System Block Diagram

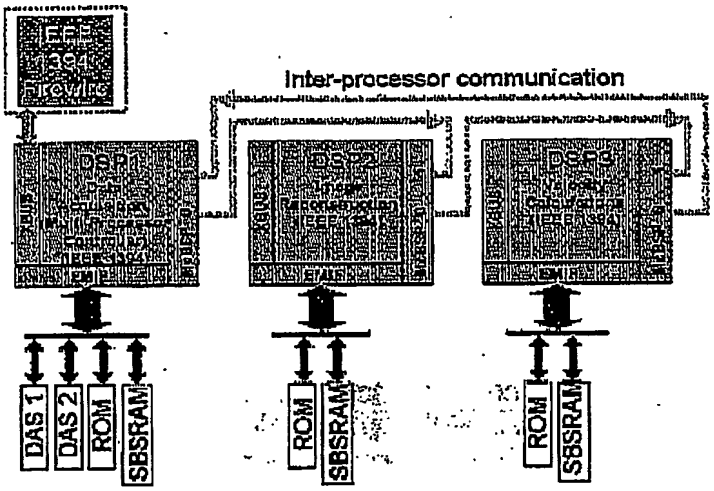

Figure 2: A diagram showing one possible system configuration of high performance two-phase flowmeter using the DSP module as a building block.

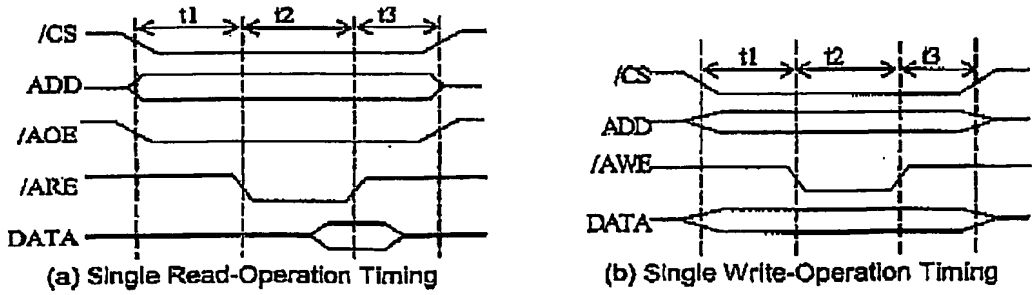

Figure 3: Interface Read-Timing And Write-Timing Where t1= 0-60ns; t2=0-262ns, t3=0-12ns. The /CS signal in Fig.2 is chip selection signal decoded from address signal EA[17:2].

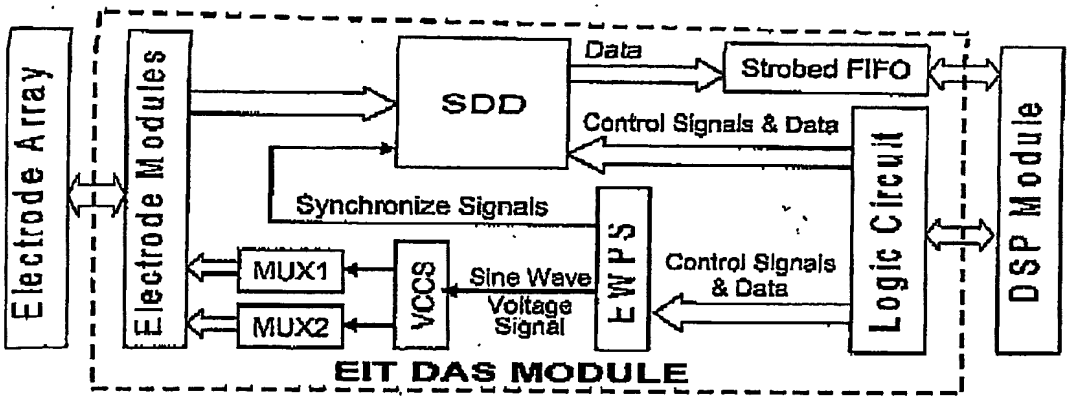

Figure 4: Architecture of EIT DAS

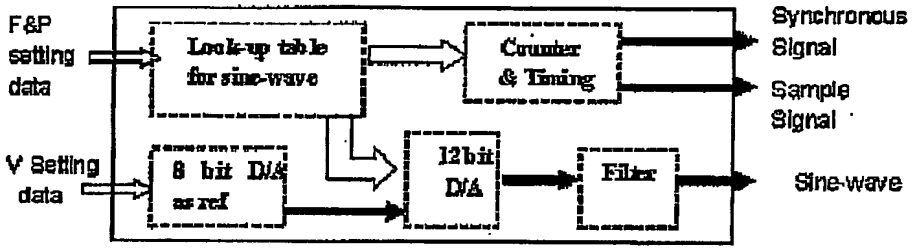

Figure 5: The structure of Equal-Width Pulse Synthesizer (EWPS)

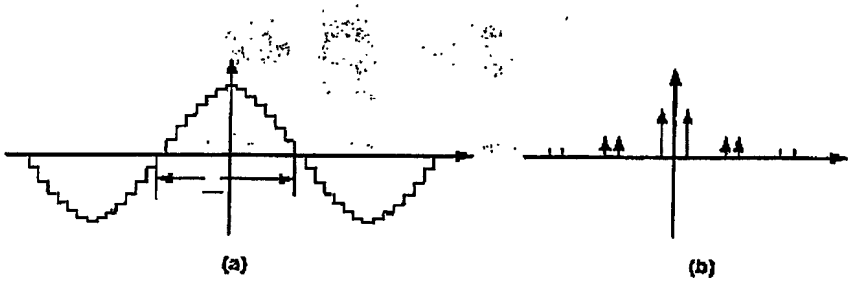

Figure 6: A staircase cosine wave (a) in time domain and (b) in frequency domain

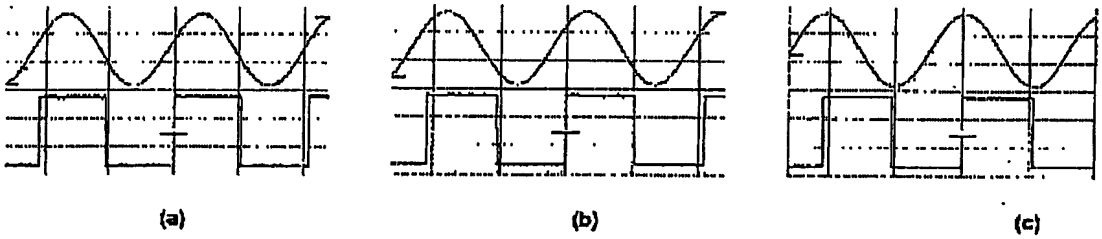

Figure 7: Programmable phase shift function (a) phase shift 15° (b) phase shift 45° (c) phase shift 90°

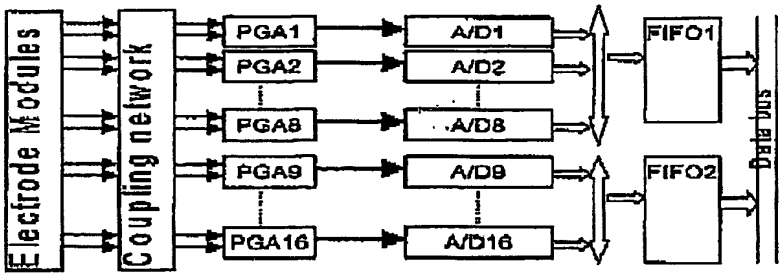

Figure 8: The structure of Synchronised Digital Demodulation (SDD)

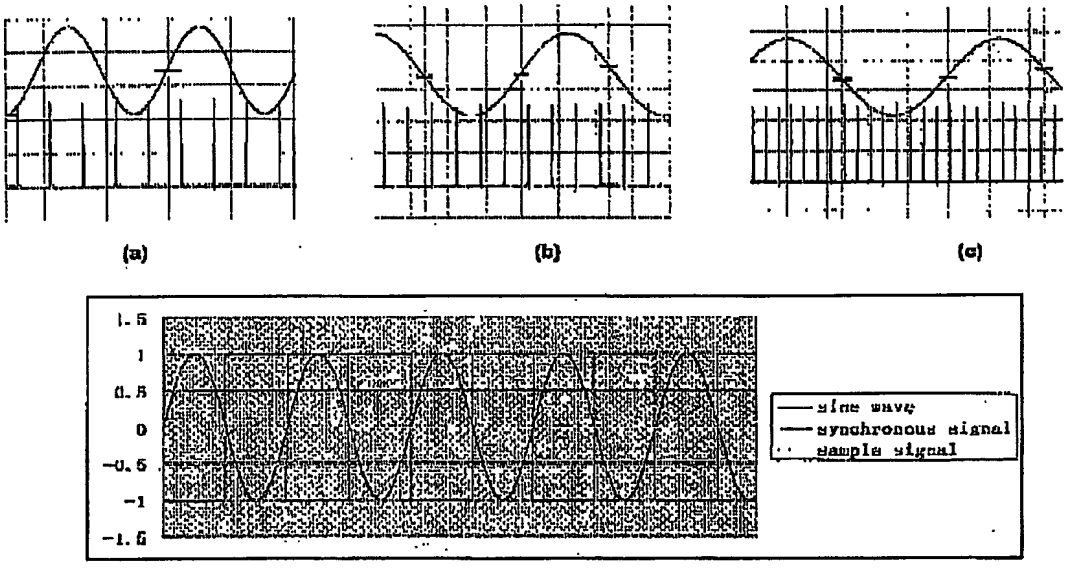

Figure 9: The configuration of the sampling modes (a) 4 samplings; (b) 8 samplings; (c) 16 samplings. (d) rolling-sample method.

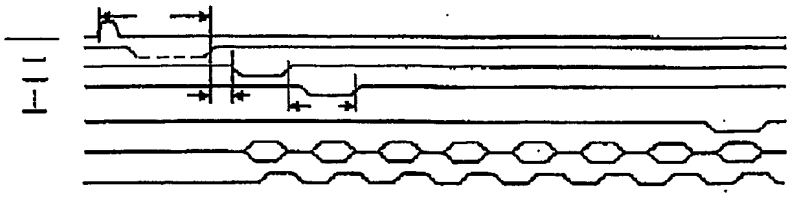

Figure 10: Reading data timing

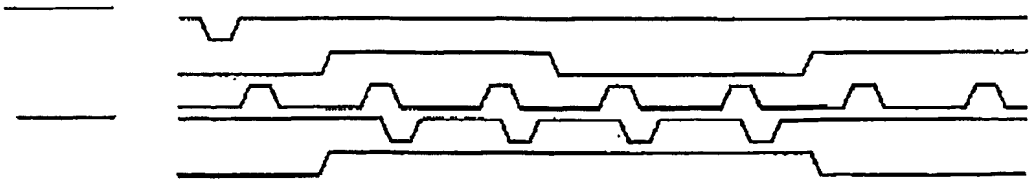

Figure 11: Sampling signal for measurement timing

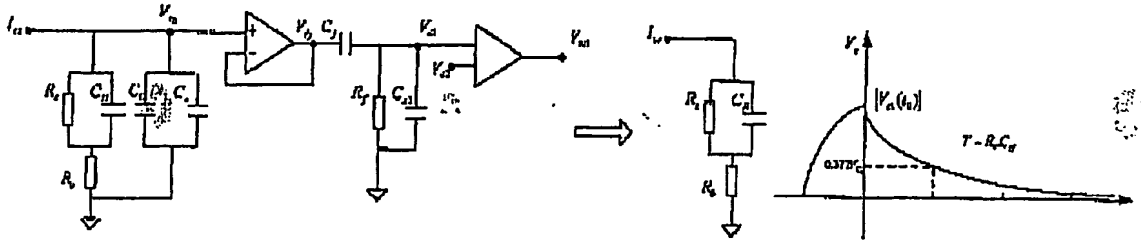

Figure12: An equivalent circuit for the EIT transducer electronics

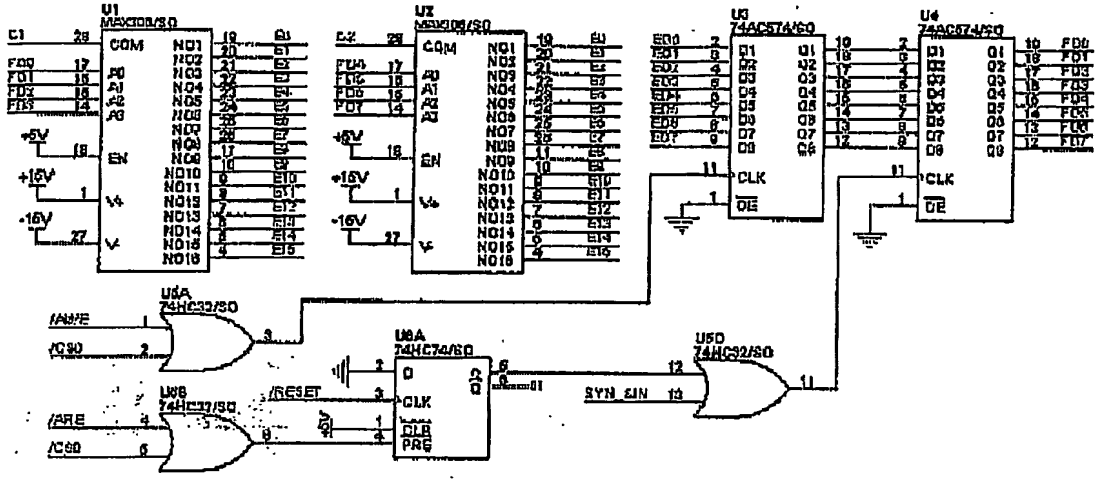

Figure 13: Realization Circuit of Over-Current-Zero Switching

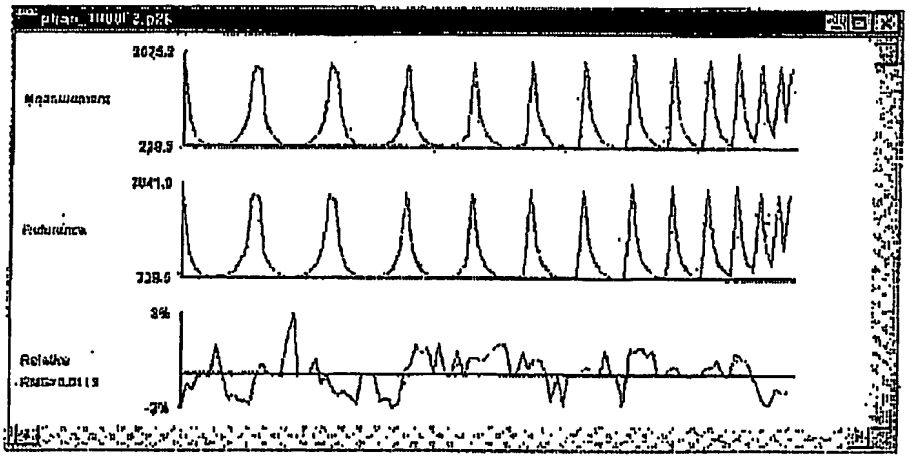

Figure 14: A typical curve of the independent measurements obtained from a 2D phantom filled with water. Data was obtained from a 2D phantom filled with mains tap water.

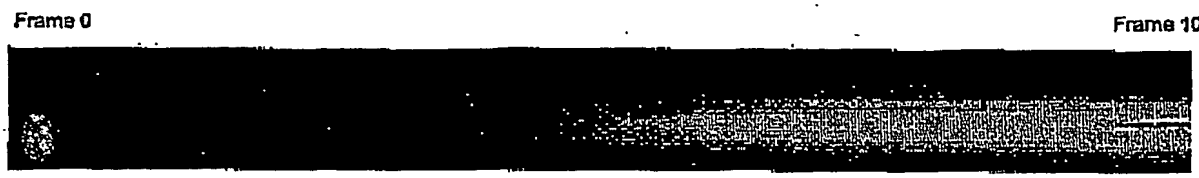

Figure 15: An axial cutting image of a high conductive droplet dropped into water, which is stacked from 1000 EIT images reconstructed using SBP algorithm. The 1000 frames of data were taken in 1.06 s